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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/619,169
Filing Date: July 14, 2003
Appellant(s): GUERRERO MERCADO, FRANCISCO JAVIER

Daniel E. Venglarik
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/16/2006 appealing from the Office action mailed 9/13/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,841,306	Lim	11-1998
6,323,695	Heinrich	11-2001

Sedra et al. "Microelectronic Circuits" 1989, pp. 220-223, 337-347.

(9 Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 7-8 and 15-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In this instant, the specification has failed to describe as to how "the pulsed bias curent comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock" of claim 7 is made and/or used. Page 13, lines 12-14 of the specification has briefly mentioned that "pulse generator produces a 390ns wide pulse on every falling edged of the clk signal, and the comparator output out is sampled with the clk signal's rising edge". Figure 3 shows a black box labeled as "Pulse Generator" 301. A careful examination of the box 301, it is noted that there is no clock signal being shown. Similarly, the comparator 100 does not show the clock signal. Therefore, it is unclear as to how the pulsed bias curent comprises a pulse at one edge of **a system clock** and an output of the comparator is sampled at **another edge of the system clock** is performed without undue experimentation.

Regarding claims 8 and 17, the specification fails to describe as to how "the comparator

selectively operates in a first mode in which the input gain stage is biased by a bias current with a defined first level value or in a second mode in which the input gain stage is biased a bias current with a different second level value" is enabled. Page 11, lines 6-25; page 12, lines 1-25 of the specification uses waveforms diagrams of figures 2A to 2C discusses the slow and fast operational modes of the comparator. Figures 4A and 4B shows the detailed structure of the comparator. **However, it is unclear as to how the circuit shown in figures 4A and 4B enable operatively in first and second modes** as called for in claim 8. That is, it is unclear as to how the comparator is selected to operate in a first mode in which the input gain stage is biased by a bias current with a defined first level value or when the comparator is selected to operate in a second mode the input gain stage is biased a bias current with a different second level value without undue experimentation.

Claims 15 and 16 are rejected for the same reasons as claims 7 and 8, respectively.

Regarding claim 19, the specification fails to describe as to how the "current source biased by the pulsed or continuous bias current and controlled by the input signal" is enabled. Figure 1 shows **"an equivalent circuit"** of the actual present invention. The equivalent circuit shows a symbol of a variable current (ibias) being received a symbolic gm signal. Page 11, lines 6-25; page 12, lines 1-25 of the specification uses waveforms diagrams of figures 2A to 2C discusses the slow and fast operational modes of the comparator. Figures 4A and 4B shows the detailed structure of the comparator. **However, it is unclear as to how the current source being biased by the pulse or continuous bias current and controlled by the input current would correspond to the actual components of the actual comparator shown in figures 4A**

and 4B. Therefore, it is unclear as to how current source biased by the pulsed or continuous bias current and controlled the input signal" is achieved without undue experimentation.

Claims 18 and 20 are rejected under 35USC 112, first paragraph because of the technical deficiencies of claim 17.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Lim (USP 5,841,306). Figure 4 of Lim shows an integrated circuit comparator comprising an input receiving an input signal (current along collector/emitter of transistors Q8, Q9) representative of a difference between quantities to be compared (Vth, Vref), an input gain stage (Q8, Q9, R7, R8) receiving the input signal and biased with a pulsed bias current (current (b) at the collector of transistor Q7, the waveform of the current is shown in figure 5C. The current (b) is pulse current), the input gain stage producing a gain based upon the input signal as called for in claims 1, 9.

Regarding claims 2 and 10, the input signal is a current representative of transconductance of a differential pair of input transistors (Q8, Q9).

Regarding claims 3 and 11, the input gain stage further comprises a current source (Q5, Q7) biased by the pulsed bias current (the current version of the Vtri at the collector of transistor

Q2) and controlled by the input signal (/Tout is the inverted version of Tout where Tout is output version of the input signal, e.g., signal along collector and emitter of Q8).

3. Claims 1-3, 8-11 and 16, 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Heinrich (USP 6,323,695).

Figure 1 of Heinrich shows an integrated circuit comparator comprising an input receiving an input signal representative of a difference between quantities to be compared (U and Vref), an input gain stage (T1, T2, T3, Sp4) receiving the input signal and biased with a pulsed bias current (Ic current signal at node S, the waveform of the current is shown in figure 3. The current is a pulse current), the input gain stage producing a gain based upon the input signal as called for in claims 1, 9 and 17.

Regarding claims 2 and 10, the input signal is a current representative of transconductance of a differential pair of input transistors (T1, T2).

Regarding claims 3 and 11, the input gain stage further comprises a current source (Sp4) biased by the pulsed bias current (Ic at node S) and controlled by the input signal (U).

Regarding claims 8 and 16, wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a bias current with a defined first level (figures 2 and 3, the constant current Ic1 at t0, t2 and t4 periods) or in a second mode in which the input gain stage is biased a bias current with a different second level value (pulsed current Ic1 at t1 and t3).

Regarding claim 17, figure 1 of Heinrich shows a comparator selectively operating in a first mode in which an input gain stage (T1, T, Sp5, Sp4) of the comparator is biased with a pulsed bias current (Ic1 is pulse in the periods t1, t3) and a second mode in which the input gain

stage is biased with a continuous bias current (constant current at periods t0, t2 and t4 are supplied to the input gain stage in a second mode of operation).

Regarding claim 18, the input gain stage receives an input (U-Vref) representing the different between U and Vref and produces a gain based upon a current for he input signal representative of transconductance of a differential pair of input transistors (T1, T2).

Regarding claim 19, figure 1 shows the input gain stage further comprises a current source (Sp4) biased by the pulsed bias current (Ic at node S) and controlled by the input signal (U).

Response to Arguments

35USC 112, first paragraph:

Regarding the rejection of claims 7-8 and 15-20 under 35USC 112, first paragraph as the specification has failed to describe in such a way to enable one skilled in the art to make and/or use of the present invention, appellant argues that the test of enablement is whether one skilled in the art could make and use of the invention from the disclosures without undue experimentation. Appellant further stated that it was well-known in the art at the time the instant application was filed that a global or "system" clock can be used to coordinately control various components or logical units within an integrated circuit. Appellant argues that such signals are understood to exists and generally are NOT depicted in high level drawings (e.g., functional unit drawings, as opposed to circuit diagrams). Thus, those skilled in the art would not be confused by the absence of a expressly depicted system clock signal within a functional drawing of an integrated circuit. Examiner respectfully traverses the above argument. Although, global or system clock signal may be used to coordinate various components in a system, it is still unclear as to how the pulsed

biased current is generated from the system clock. This pulsed biased current is being used to bias the input gain stage, one of the inventive features of the present invention, thus providing a gain. The specification briefly mentions the pulse current is produced (page 13, lines 12-14). Since the pulsed current bias is a critical feature of the present invention, it is considered an undue experimentation for one skilled in the art to have to determine how to produce a pulse generator that are capable of generating the pulsed current bias as disclosed in the specification. Therefore, the rejection is deemed proper.

Appellant argues that the application of current Ib of Lim et al. reference and Ic of Heinrich reference to anticipate the "pulsed bias current" is contradictory with the rejection of claims 7 and 15 under 35 USC 112, first paragraph is not persuasive. Claims 1-3 and 10-11 (anticipated by Lim); 1-3, 8-11 and 16, 17 (Heinrich) do not call for the pulsed bias current generated in associated with the system clock and the output comparator. Therefore, claims 7-8 and 15-20 remain rejected under 35USC 112, first paragraph.

Regarding the rejection of claims 8 and 17, appellant points out sections of page 11, in particular, paragraph 0023 to support the recited limitations of claims 8 and 17. Paragraph 0023 states there are two modes of operation, i.e., low speed mode and high speed mode. Each mode of operation is driven with different bias current values. However, the specification fails to describe as to how the mode of operation is selected. Therefore, it would be undue experimentation for one skilled in the art to try to determine how to make a comparator whose bias current is at different level in different mode of operation. Therefore, the rejection is deemed proper.

Regarding the rejection of claim 19 as being non-enablement, appellant points to figure 1 showing the equivalent circuit of figure 1 and concludes that no undue experiment would be required for those skilled in the art to implement the features of claim 19 is not persuasive. Figure 1 shows a parameter gm as a pulse controlling the current source (I1) for producing a pulsed or continous bias current. However, the appellant fails to point out as how to implement a circuit in which the **parameter** gm is generated and a current source is controlled by the **parameter** gm in producing the pulsed or continuous bias current. Therefore, it is unclear as to how current source biased by the pulsed or continuous bias current and controlled the input signal" is achieved without undue experimentation.

Therefore, the rejection of claims 7-8 and 15-20 under 35USC 112, first paragraph is deemed proper.

35USC 102(b) as being anticipated by Lim (USP 5,841,306):

Regarding claims 1-3 and 10-11 as being anticipated by Lim (USP 5,841,306), appellant argues that Lim "does not teach providing a pulsed bias current-that is, a current that is pulsed in accordance with a system clock" is not persuasive. The independent claims 1 and 9 do not call for pulsed bias current-that is, a current that is pulsed in accordance with a system clock. Appellant also argues Lim et al.'s figure 5c shows a continous bias current instead of a pulsed bias current is incorrect. Figure 5c clearly shows a pulse shape waveform. Therefore, the limitation of pulsed bias current is fully met.

Regarding claims 2 and 10, appellant argues that Lim does not show the input signal as a current representative of transconductance of a differential pair of input transistors is not persuasive. Sedra et al. clearly proves that transconductance parameter is directly proportional to

the collect current of a bipolar transistor. Thus, the collector current along collect-emitter path of the input transistors Q8 and Q9 is the input signal (gm). Therefore, the limitations of claims 2 and 10 are fully met.

35USC 102(b) as being anticipated by Heinrich (USP 6,323,695):

Regarding the rejection claims 1-3, 8-11 and 16-17 as being anticipated by Heinrich (USP 6,323,695), appellant argues that Heinrich show a continous bias current at varying levels depending on an operating mode is not persuasive. The current Ic1 in figure 3 has a pulse shape waveform therefore anticipates the pulse bias current limitations as called for in claims 1, 9 and 17. Therefore, the rejection is deemed proper.

Regarding claims 2 and 10, appellant argues that Heinrich does not show the input signal as a current representative of transconductance of a differential pair of input transistors is not persuasive. Sedra et al. clearly proves that transconductance parameter is directly proportional to the drain current of a field effect transistor. Thus, the drain current along drain-source path of the input transistors T1 and T2 is the input signal (gm). Therefore, the limitations of claims 2 and 10 are fully met.

Regarding claims 16-17, appellant argues that Heinrich does not show the comparator selectively operates in a first mode in which the input gain stage is biased by continous bias current **or (emphasis added)** in a second mode in which the input stage is biased by pulsed bias current is not persuasive. Figure 3 shows the waveform of the current Ic1 over five periods (t0 to t4). In a first mode of operation the input gain stage is biased with a bias current having a defined first level (figures 2 and 3, the current Ic1 is constant (continous) at t0, t2 and t4 periods) or in a second mode in which the input gain stage is biased with bias current having a different

second level value (the current Ic1 is pulsing between high and low levels in periods t1 and t3). Therefore, the limitations of claims 16-17 are fully met.

Allowable Subject Matter

4. Claims 4-6 and 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Conferees:

Timothy Callahan, SPE.

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Tuan T. Lam, Primary Examiner.